What is claimed is:

CLAIMS

1. A method for operating a transmitter to transmit data, the method comprising the steps of:

reading one or more bits;

determining a first cyclical shift based on a bit pattern of the one or more bits;

obtaining a first direct sequence spread spectrum code characterized by the first cyclical shift; and

transmitting the first direct sequence spread spectrum code.

2. The method according to claim 1, wherein:

the step of reading a plurality of bits comprises the sub-step of:

reading N bits; and

the step of obtaining a 2^N element first direct sequence spread spectrum code that includes an M-sequence and one or more appended zeros.

3. The method according to claim 1 wherein the step of obtaining a first direct sequence spread spectrum code characterized by the first cyclical shift state comprises the sub-steps of:

reading the first direct sequence spread spectrum code in a state characterized by a second cyclical shift; and

cyclically shifting the first direct sequence spread spectrum code.

4. The method according to claim 1 wherein the step of obtaining a first direct sequence spread spectrum code characterized by a first cyclical shift comprises the sub-step of:

reading the first direct sequence spread spectrum code from a memory.

5. The method according to claim 1 wherein the step of transmitting the first direct sequence spread spectrum code comprises the sub-step of:

transmitting the first direct sequence spread spectrum code in a first channel of a phase shift key signal.

6. The method according to claim 1 further comprising the step of:

transmitting a second direct sequence spread spectrum code.

7. The method according to claim 1 wherein:

the step of transmitting the first direct sequence spread spectrum code comprises the sub-step of:

transmitting the first direct sequence spread spectrum code in a first channel of a quadrature phase shift key signal; and

the step of transmitting the second direct sequence spread spectrum code comprises the sub-step of:

transmitting the second direct sequence spread spectrum code in a second channel of the quadrature phase shift key signal.

8. A method for operating a receiver, the method comprising the steps of:

receiving a signal that includes a first direct sequence spread spectrum code;

determining a correct relative cyclical shift of the first direct sequence spread spectrum code; and

outputting one or more bits having a bit pattern associated with the correct relative cyclical shift.

9. The method according to claim 8 wherein the step of determining a correct relative cyclical shift comprises the sub-step of:

performing a dot product operation between the first direct sequence spread spectrum code and a reference code at a plurality of relative cyclical shifts to obtain a plurality of dot product values.

10. The method according to claim 9 wherein the step of determining a correct relative cyclical shift further comprises the sub-step of:

testing one or more inequality relations involving each of the plurality of dot product values in order to identify the correct cyclical shift that corresponds to a first dot product value from the plurality of dot product values that passes one or more inequality relations.

11. The method according to claim 8 wherein the step of receiving a signal comprises the sub-step of:

receiving a signal that includes the first direct sequence spread spectrum code, and a second direct sequence spread spectrum code.

12. The method according to claim 11 wherein the step of receiving a signal comprises the sub-step of:

receiving a quadrature phase shift key signal including the first direct sequence spread spectrum code in a first channel, and a second direct sequence spread spectrum code in a second channel.

13. The method according to claim 11 wherein the step of determining a correct relative cyclical shift comprises the sub-step of:

determining the correct relative cyclical shift of the first direct sequence spread spectrum code relative to the second direct sequence spread spectrum code.

14. The method according to claim 13 wherein the step of determining a correct relative cyclical shift comprises the sub-step of:

performing a dot product operation between the first direct sequence spread spectrum code and a first reference code at a plurality of relative cyclical shifts to obtain a first plurality of dot product values;

testing one or more inequality relations involving each of the first plurality of dot product values in order to identify a first relative cyclical shift which corresponds to a first dot product value from the plurality of dot product values that passes at least one inequality relation among the one or more inequality relations;

performing a dot product operation between the second direct sequence spread spectrum code and a second reference code at a plurality of relative cyclical shifts to obtain a second plurality of dot product values;

testing one or more inequality relations involving each of the second plurality of dot product values in order to identify a second relative cyclical shift which corresponds to a first dot product value from the plurality of dot product values that passes at least one inequality relation among the one or more inequality relations; and

subtracting the first relative cyclical shift from the second relative cyclical shift to obtain the correct relative cyclical shift.

15. The method according to claim 8 wherein the step of receiving a signal comprises the sub steps of:

demodulating the signal using a quadrature demodulator; and

sampling the signal to obtain a sequence of complex chip values including the first direct sequence spread spectrum code.

16. The method according to claim 15 further comprising the step of:

multiplying each Nth complex chip value in the series of complex chip values by a (N+K)th complex chip value in the series of complex chip values that is separated from the Nth complex chip value by a K places to obtain a decoded sequence.

17. The method according to claim 16 wherein the step of determining a correct relative cyclical shift comprises the sub-step of:

performing a dot product operation between the decoded sequence and a reference code at a plurality of relative cyclical shifts to obtain a plurality of dot product values; and

testing one or more inequality relations involving each of the plurality of dot product values in order to identify the correct cyclical shift that corresponds to a first dot product value from the plurality of dot product values that passes one or more inequality relations.

18. A spread spectrum transmitter comprising:

a bit pattern encoder for receiving one or more bits at an input and outputting a predetermined relative cyclical shift value in response to each possible bit pattern of the one or more bits at an output; and

a cyclical shifter for receiving the relative cyclical shift value at an input and outputting a first spread spectrum code that has been shifted by the predetermined cyclical shift value at a cyclical shifter output.

19. The spread spectrum transmitter according to claim 18 further comprising:

a modulator including a first modulator input for receiving a first baseband signal including first spread spectrum code that has been shifted by the predetermined cyclical shift value.

20. The spread spectrum transmitter according to claim 19 further comprising:

a first pulse shaper for receiving the first spread spectrum code that has been shifted by the predetermined cyclical shift value at a first pulse shaper input that is coupled to the cyclical shifter output and outputting the first baseband signal based on the first spread spectrum code that has been shifted by the predetermined cyclical shift value at a first pulse shaper output that is coupled to the first modulator input.

21. The spread spectrum transmitter according to claim 20 wherein the modulator further comprises:

a second modulator input for receiving a second baseband signal.

22. The spread spectrum transmitter according to claim 21 further comprising:

a second pulse shaper for outputting the second baseband at a second pulse shaper output that is coupled to the second modulator input, in response to receiving a second spread spectrum code at a second pulse shaper input; and

a memory for storing the second spread spectrum code including a memory output coupled to the second pulse shaper input.

23. A spread spectrum transmitter comprising:

a processor programmed to:

read binary data;

parse the binary data into a plurality of groups of N bits;

select a cyclical shift based on a bit pattern of each of the plurality of groups of N bits; and

generate a cyclically shifted spread spectrum code by cyclically shift a first spread spectrum code by the cyclical shift .

24. The spread spectrum transmitter according to claim 23 wherein the processor is further programmed to:

generate a digital representation of a first baseband signal that includes the cyclically shifted spread spectrum code.

25. The spread spectrum transmitter according to claim 24 further comprising:

a first digital to analog converter coupled to the processor for receiving the digital representation of the first baseband signal and outputting a first analog baseband signal; and

a modulator including a first input coupled to the first digital to analog for receiving the first analog baseband signal and modulating a carrier wave with the first analog baseband signal.

26. The spread spectrum transmitter according to claim 25 wherein the processor is programmed to:

generate a digital representation of a second baseband signal; and

the transmitter further comprises:

a second digital to analog converter coupled to the processor for receiving the digital representation of the second baseband signal and outputting a second analog baseband signal; and

the modulator includes:

a second input coupled to the second digital to analog for receiving the second analog baseband signal and modulating the carrier wave with the second analog baseband signal.

27. A spread spectrum receiver comprising:

a first correlator for determining a relative cyclical shift of a first received spread spectrum code; and

a relative shift to bit pattern decoder for outputting the identity of an information symbol based on the relative cyclical shift of the received spread spectrum code.

28. The spread spectrum receiver according to claim 27 further comprising:

a second correlator for determining a relative cyclical shift of a second received spread spectrum code; and

a time comparer for determining the relative cyclical shift of the first received spread spectrum code with reference to the relative cyclical shift of the second received spread spectrum code.

29. The spread spectrum receiver according to claim 28 further comprising:

a quadrature phase shift key demodulator for demodulating a signal that includes the first received spread spectrum code and the second received spread spectrum code, and outputting a series of complex chip values at an in-phase output and a quadrature phase output.

30. The spread spectrum receiver according to claim 29 further comprising;

a complex chip multiplier including:

a first input coupled to the in-phase output, and a second input coupled to the quadrature-phase output

for receiving the series of complex chip values and multiplying each Nth complex chip value in the series of complex chip values by a (N+K)th complex chip value in the series of complex chip values that is separated from the Nth complex chip value by a K places to obtain a decoded sequence to obtain a differentially decoded series.

31. The spread spectrum receiver according to claim 28 wherein the first correlator comprises:

a shift register including:

a first serial input for receiving the differentially decoded series; and

a first parallel output;

a first dot product operator including:

a first parallel input coupled to the first parallel output;

a second parallel input; and

a first dot product operator output; and

a reference first code memory including:

an first memory output coupled to the second parallel input; and

a first comparator including:

a first input coupled to the output; and

a second input;

a threshold value source coupled to the second input; and

a first comparator output;

32. The spread spectrum receiver according to claim 31 wherein the second correlator comprises:

a shift register latch including a

a second serial input for receiving the differentially decoded series;

a second parallel output; and

a control input coupled to the first comparator output; and

a second dot product operator including:

a third parallel input coupled to the second parallel output;

a fourth parallel input; and

a second dot product operator output; and

a second reference code memory including:

a second memory output; and

a cyclical shifter including:

a fifth parallel input coupled to the second output; and

a third parallel output coupled to the fourth parallel input; and

a second comparator including:

a first input coupled to the second dot product operator output;

a second input coupled to a threshold value source; and

a second comparator output.

33. The spread spectrum receiver according to claim 32 wherein the time comparer includes:

a first input coupled to the first comparator output, and

a second input coupled to the second comparator output.

34. A spread spectrum receiver comprising:

a processor programmed to:

determine a first relative cyclical shift of a first received cyclically shifted spread spectrum code; and

output an information symbol associated with the first relative cyclical shift.

35. The spread spectrum receiver according to claim 34 wherein

the processor is programmed to:

correlate the first received cyclically shifted spread spectrum code with a first reference code;

correlate a second received spread spectrum code with the first reference code.

determine the first relative cyclical shift relative to the second received spread spectrum code.

36. A computer readable medium containing programming instructions for operating a transmitter, the computer readable medium including programming instructions for:

reading one or more bits;

determining a first cyclical shift based on a bit pattern of the one or more bits;

obtaining a first direct sequence spread spectrum code characterized by the first cyclical shift; and

transmitting the first direct sequence spread spectrum code.

37. A computer readable medium including programming instructions for operating a receiver, the computer readable medium including programming instructions for:

receiving a signal that includes a first direct sequence spread spectrum code;

determining a correct relative cyclical shift of the first direct sequence spread spectrum code; and

outputting one or more bits having a bit pattern associated with the correct relative cyclical shift.

38. A communication system comprising:

a transmitter including:

a bit pattern encoder for receiving one or more bits at an input and outputting a predetermined relative cyclical shift value in response to each possible bit pattern of the one or more bits at an output;

a cyclical shifter for receiving the relative cyclical shift value at an input and outputting a first spread spectrum code that has been shifted by the predetermined cyclical shift value at a cyclical shifter output; and

a receiver including:

a first correlator for determining a relative cyclical shift of the first spread spectrum code; and

a relative shift to bit pattern decoder for outputting the identity of an information symbol based on the relative cyclical shift of the received spread spectrum code.